WHAT IS CLAIMED IS:

1. A semiconductor device comprising a driver circuit for driving a voltage at an output node in accordance with an input signal received at an input node, wherein

said driver circuit includes:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with a voltage level of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off complementarily to said first transistor in accordance with a voltage of a second internal node; and

a control circuit controlling voltages of said first and second internal nodes so as to complementarily turn on said first and second transistors in accordance with said input signal,

said control circuit has a voltage adjustment circuit connected to at least one of said first and second internal nodes, and

when one of said first and second transistors corresponding to the internal node connected to said voltage adjustment circuit is turned on in accordance with the voltage level of the connected internal node, said voltage adjustment circuit sets the voltage of said connected internal node at a voltage level different from the voltage levels of said first and second voltages.

2. The semiconductor device according to claim 1, wherein

the voltage of said connected internal node is set at one of said first and second voltages when the corresponding transistor is turned on.

3. The semiconductor device according to claim 1, wherein

said control circuit further has a timing circuit provided in correspondence with said at least one of said first and second internal nodes, and

when the corresponding transistor is turned on, said timing circuit

connects one of said first and second voltages for turning on said corresponding transistor to said connected internal node for a predetermined period.

4. The semiconductor device according to claim 3, wherein

said timing circuit adjusts said predetermined period in accordance with the voltage of said output node.

5. The semiconductor device according to claim 3, wherein

said timing circuit has a delay circuit for delaying said input signal, and

said predetermined period corresponds to delay time given by said delay circuit.

6. The semiconductor device according to claim 1, wherein

said control circuit sets the internal node of the other of said first and second transistors at one of said first and second voltages for turning on said corresponding transistor so as to turn off said other transistor when said corresponding transistor is turned on, and

said control circuit further has a connection circuit for electrically connecting said first internal node and to said second internal node for a predetermined period when the corresponding transistor is turned on.

7. The semiconductor device according to claim 6, wherein

said connection circuit has a delay circuit delaying said input signal, and

said predetermined period corresponds to delay time given by said delay circuit.

8. The semiconductor device according to claim 1, wherein

said first and second transistors are each constituted by a field effect transistor having a gate oxide film, and

said semiconductor device further comprises another field effect

transistor having a different gate oxide film from said gate oxide film of at least one of said first and second transistors.

9. The semiconductor device according to claim 1, wherein

said first and second transistors are each constituted by a field effect transistor having a dielectric film, and

said semiconductor device further comprises another field effect transistor having a different dielectric film from said dielectric film of said at least one of said first and second transistors.

10. The semiconductor device according to claim 1, wherein

said input signal includes a plurality of signals, and

said control circuit controls the voltages of said first and second internal nodes in accordance with a predetermined logic operation result based on said plurality of signals.

11. The semiconductor device according to claim 10, wherein

said control circuit further has a timing circuit provided on at least one of said first and second internal nodes, and

said timing circuit connects one of said first and second voltages for turning on said corresponding transistor to said connected internal node for a predetermined period when the corresponding transistor is turned on.

12. A semiconductor device comprising a driver circuit for driving a voltage at an output node in accordance with an input signal received at an input node, wherein

said driver circuit includes:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with a voltage level of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off in accordance with a voltage level of a second internal node;

a third transistor connected in parallel to said second transistor between said output node and said second voltage, and turned on and off, complementarily to said first transistor, in accordance with the voltage level of said first internal node; and

a control circuit for controlling voltages of said first and second internal nodes so as to complementarily turn on said first transistor and said second and third transistors in accordance with said input signal,

said control circuit sets one of said first and second voltages for turning on said second and third transistors to said first internal node so as to turn off said first transistor when said second and third transistors are turned on, and supplies said one of said first and second voltages to said second internal node for a predetermined period, and

said second transistor has a driving force for supplying said second voltage to said output node higher than that of said third transistor.

13. The semiconductor device according to claim 12, wherein

said control circuit has a timing circuit provided in correspondence with said second internal node, and

said timing circuit adjusts said predetermined period in accordance with the voltage level of said output node.

14. The semiconductor device according to claim 12, wherein

said control circuit has a connection circuit for electrically connecting said first internal node to said second internal node for said predetermined period.

15. The semiconductor device according to claim 12, wherein

said input signal includes a plurality of signals, and

said control circuit controls the voltages of said first and second internal nodes in accordance with a result of a predetermined logic operation performed based on said plurality of signals.

16. The semiconductor device according to claim 12, wherein

each of said first, second and third transistors is formed of a field-effect transistor having a gate oxide film, and

said semiconductor device further comprises another field-effect transistor having a different gate oxide film from said gate oxide film of at least one of said first, second and third transistors.

17. The semiconductor device according to claim 12, wherein

said control circuit includes a noise adjustment circuit for supplying one of said first and second voltages for turning on said second and third transistors to said first internal node in response to an external instruction in a standby state.

18. A semiconductor device comprising a first driver circuit and a second driver circuit arranged to be adjacent each other, each of the first and second driver circuits driving a voltage at an output node in accordance with an input signal received at an input node, wherein

each of said first and second driver circuits includes:

a first transistor connected between a first voltage and said output node, and turned on and off in accordance with a voltage level of a first internal node;

a second transistor connected between said output node and a second voltage, and turned on and off in accordance with a voltage level of a second internal node;

a third transistor connected in parallel to said second transistor between said output node and said second voltage, and turned on and off, complementarily to said first transistor, in accordance with the voltage level of said first internal node; and

a control circuit for controlling voltages of said first and second internal nodes so as to complementarily turn on said first transistor and said second and third transistors in accordance with said input signal,

said control circuit of each of said first and second driver circuits sets one of said first and second voltages for turning on said second and third transistors to said first internal node so as to turn off said first transistor

when said second and third transistors are turned on, and supplies said one of the first and second voltages to said second internal node for a predetermined period,

said second transistor has a driving force for supplying said second voltage to said output node higher than that of said third transistor, and

said control circuit of each of said first and second driver circuits includes a noise adjustment circuit for supplying one of said first and second voltages for turning on said second and third transistors to said second internal node in accordance with the input signal inputted to the adjacent driver circuit in a standby state.